

ABSTRACT

[212] A system and method for the simulation of discrete events. Events can be defined or mapped from Boolean logic, finite equations, lookup tables, emulation of processors, or may be algebraic in nature. An event-based simulation scheme with single-memory word representation of event models and timing is described. Event models are instantiated in parallel simulator engines (logic, behavioral, soft-emulation, memory, processor, interconnection, and/or any combination of these). A central scheduler minimizes computation time traditionally spent on sorting chronology and sequence of events as the events propagate through models and interconnections or links, with the scheduler interfaced to each engine via dedicated pipelined communications channels. The scheduler simultaneously serves pending events to simulation engines for evaluation and retrieves future events from these engines for sorting and resubmitting for further simulation. The simulator scheduler addresses simulator cycle time management, sub-cycle event handling (new pending events), and the recording of results. The capacity of simulator preferably exceeds multi-millions of models and the computational speed approaches multi-millions of events per second.